REMARKS

Prior to the present amendment, claims 1-10 were pending in the application. Claim 1 is amended above. Claim 10 is canceled above. Claims 1-9 are now pending the present application. No new matter is added by the claim amendment. Entry is respectfully requested.

Claims 1-10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ejiri (U.S. Patent No. 6,770,974) in view of Applicant Admitted Prior Art (AAPA). Reconsideration and removal of the rejections are respectfully requested.

In the present invention as claimed in amended independent claim 1, the "electrode lines comprise one of word lines and bit lines of the semiconductor device." This limitation is incorporated into claim 1 from former claim 10, now canceled. The "electrode lines" each include a "first line unit" that functions as an electrode line, and a "second line unit" that includes the inclined outer end and is separated from, and insulated from, the first line unit by an insulating plug. This feature is illustrated at FIG. 4 of the present specification. In this example, the electrode lines 130 are formed on an upper portion of a semiconductor substrate 100, and may comprise word lines or bit lines (see FIG. 4 and page 5, lines 18-22 of the present specification). Word lines and bit lines are commonly employed in contemporary highly integrated memory devices, and the characteristics of such devices are closely related to the line width of the word lines and bit lines of the devices.

As described in detail in previous responses filed by the Applicant during prosecution of the present application, Ejiri teaches the formation and structure of capacitive elements. Certain embodiments of the electrodes of the capacitive elements of Ejiri incidentally have a tapered surface that is at an intermediate region of the Ejiri dummy electrode. Indeed, many integrated devices have portions that are tapered as various upper layers are applied to the devices.

The teachings of the AAPA in the Background section of the present application illustrate the formation of electrode lines, for example bit lines or word lines of a memory device, and further illustrate the problem that occurs at the extreme ends of the lines.

What is claimed in the present invention as claimed in amended claim 1 is an "electrode line structure of a semiconductor device", where electrode lines comprising one of word lines and bit lines have inclined outer ends that are a result of their formation. The electrode lines, comprising one of bit lines and word lines, as claimed in claim 1 of the present invention, are much different in structure than the Ejiri capacitor electrode. Bit lines and word lines of a semiconductor device tend to be formed over an entire length of a cell array of a memory device, as a given line serves multiple rows or columns of cells of a given device, and therefore such lines are relatively long in length. Their long and narrow structure allows for greater efficiency in more densely populating the memory cell region of a semiconductor device.

A capacitor electrode of the type described in connection with the Ejiri reference, on the other hand, is much shorter in length and is configured to serve the operation of a single capacitive element. Shorter electrode structures are more desirable, to prevent the capacitor structure from occupying too large of an amount of area on the integrated device.

To establish a prima facie case of obviousness, the prior art reference or references, when combined, must not only teach or suggest all the recitations of the claim, there must also be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. To support combining references, evidence of a suggestion, teaching, or motivation to combine must be clear and particular, and this requirement for clear and particular evidence is not met by broad and conclusory statements about the teachings of the reference. To support combining or modifying references, there must be particular evidence from the prior art

as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed.

The applicants respectfully submit that the present rejection of former claim 10 set forth in the Office Action fails to meet the requirements for combining the references in the manner relied on to show obviousness. Furthermore, there is no motivation taught or suggested by either reference to make the cited combination. This is to be expected, since the two references are concerned with different technologies. Given their divergent teachings, neither reference would be expected by one of skill in the art to suggest a motivation for combination with the other, and, there is no such motivation taught or suggested by either reference.

The Applicant respectfully believes that the combination of Ejiri with AAPA is improper under 35 U.S.C. § 103(a). Specifically, there is no explicit teaching or suggestion in Ejiri that would motivate one skilled in the art to apply the Ejiri capacitor electrode structure to a word line or bit line of a semiconductor device. While the capacitive elements of Ejiri, and the word and bit lines of conventional memory devices, are both found in integrated semiconductor devices, they are from discrete areas of integrated device technology that only marginally overlap. The Ejiri dummy electrode is formed for compensating for a level difference in subsequent layer formation of a multiple-layered capacitor. Such level difference compensation is not of concern in memory device word line and bit line formation, and therefore a designer of devices employing word lines and bit lines would not be motivated to apply the Ejiri teaching to address the problems that exist at the extreme ends of word lines and bit lines of semiconductor devices.

It is submitted that Ejiri fails to teach or suggest "the electrode lines comprise one of word lines and bit lines of the semiconductor device" and "wherein the electrode lines each include a first line unit, which substantially functions as an electrode line, a second line unit, which includes the inclined outer end in the long axis direction and which is separated from the first line unit by a predetermined distance, and an insulating plug, which is interposed between the first line unit and the second line unit and electrically insulates the first line unit from the

second line unit, an upper surface of the second line unit being of uniform height above the substrate over the entire length of the second line unit between the insulating plug and the inclined outer end", as claimed in amended claim 1 of the present invention. Ejiri does not teach or suggest forming electrode lines comprising one of bit lines and word lines to have first and second line units that are separated from each other and insulated from each other by an insulative plug, in this manner. Ejiri is not involved with bit lines and word lines of semiconductor devices.

With regard to AAPA, it is submitted that AAPA, like Ejiri, fails to teach or suggest the stated limitations. In particular AAPA, like Ejiri, fails to teach or suggest "wherein the electrode lines each include a first line unit, which substantially functions as an electrode line, a second line unit, which includes the inclined outer end in the long axis direction and which is separated from the first line unit by a predetermined distance, and an insulating plug, which is interposed between the first line unit and the second line unit and electrically insulates the first line unit from the second line unit, an upper surface of the second line unit being of uniform height above the substrate over the entire length of the second line unit between the insulating plug and the inclined outer end", as claimed in amended claim 1 of the present invention.

Accordingly, it is submitted that the combination of Ejiri and AAPA fails to teach or suggest the invention set forth in independent claim 1. Since the combination of Ejiri and AAPA fails to teach or suggest the invention set forth in claim 1, the claim is believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection under 35 U.S.C. 103(a) based on the combination of Ejiri and AAPA, and allowance of amended independent claim 1, are therefore respectfully requested. With regard to dependent claims 2-9, it follows that these claims should inherit the allowability of independent claim 1 from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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